WHAT IS CLAIMED IS:

1. An image capturing device comprising:

a first solid image capturing element having a first plurality of light receiving pixels, for storing information charge which is generated in response to a first object image, in the first plurality of light receiving pixels;

a second solid image capturing element having a second plurality of light receiving pixels, for storing information charge which is generated in response to a second object image, in the second plurality of light receiving pixels;

a driving control circuit for controlling operation of the first and second solid image capturing elements; and

a register for storing first and second setting data which respectively designate driving condition for the first and second solid image capturing elements,

wherein

the driving control circuit drives the first and second solid image capturing elements respectively according to the first and second setting data stored in the register.

2. The image capturing device according to claim 1, wherein the register comprises a memory region sectioned into a plurality of blocks for respectively storing the first and second setting data.

3. The image capturing device according to claim 1, wherein the driving control circuit comprises a timing control circuit for

determining timing for conducting vertical and horizontal scanning relative to the first and second solid image capturing elements and generating a first timing signal and a second timing signal, a first driving circuit for driving the first solid image capturing element in response to the first timing signal, and a second driving circuit for driving the second solid image capturing element in response to the second timing signal, and the first driving circuit and second driving circuit are constructed such that driving capabilities thereof are respectively switchable and driving capabilities thereof to be employed are determined according to the first and second setting data, respectively.

4. The image capturing device according to claim 3, wherein the timing control circuit comprises a counter for counting a predetermined reference clock, a decoder for decoding an output from the counter to thereby create the first timing signal and the second timing signal, and a delay circuit for delaying the first timing signal and the second timing signal by a period of time which is changeable, wherein the delay circuit determines the period of time by which to delay, according to the first and second setting data.